CV of Dr. H. Fatih Uğurdağ

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HIGHLIGHTS

► Assistant Professor at **Özyeğin University** EEE & CS Dept.s (formerly at Bahçeşehir University EEE & CS)
Consultant at **Vestel Vestek** in İTÜ Teknokent since 2007 ◄
► 13 years of full-time (plus 2 years of part-time) industry employment in the US (7 years in **Silicon Valley**)
Acted as a consultant for **TCDD** (2009-10), Iontek (2009), Synplicity (2006-07), **FordOtosan** (2006), Intersil (2006), ŞişeCam (1996-97) ◄
► Research & engineering expertise spans **Embedded Systems**, ITS, ASIC/SOC/FPGA design/automation, Computer vision, E-learning
PI of a 2-year **$100K TÜBİTAK-1001** project on Analog Clock Tree Synthesis in collaboration with Boğaziçi EEE and Intersil in Silicon Valley ◄
► Co-PI of a 3-year **$250K TÜBİTAK-1001** project for developing an FPGA based DAQ with applications at MIT and CERN (PI at Boğaziçi Physics)
4 journal papers (plus 2 in preparation) and 22 conference papers ◄
► Teaching experience includes courses on Embedded systems, HDLs, VLSI design, Computer arithmetic, Datacom, Machine vision, OS
Teaching interests include Digital design, Data structures, Analysis of algorithms, Graph theory, Compiler design, Parallel processing ◄
► Taught **courses on 16 different subjects** in 14 semesters (average load of 10 lecture hrs per week and 100+ students per semester)
Taught 3 times a senior course named Pillars of Computing at Boğaziçi Physics to an audience including top engineering students ◄
► Oversaw **7 MS theses** and **64 senior projects** to completion, co-advised 2 MS theses (1 at Boğaziçi), and jury of 1 PhD thesis (at Sabancı)
Established Digital systems, Circuits labs and helped establish Embedded systems, Robotics/vision, Automation labs at Bahçeşehir & Özyeğin ◄
► Started Bahçeşehir Robotics Team in Summer 2005. Acted as advisor non-stop. They won many awards including ones at İTÜro and ODTÜ
Helped establish an undergraduate program/department in Mechatronics Engineering at Bahçeşehir University ◄
► **Associate Chairman** of the Computer Engineering Department at Bahçeşehir University in 2008-09 academic year
Established a graduate program module called MSEVS (**Embedded Video Systems**) in EEE & CMPE in collaboration with Vestel Vestek ◄
► As the program coordinator, admitted 28 students to MSEVS in 2 years. Most were top students in their undergraduate class (see ugurdag.com)
Alma maters of MSEVS students include İTÜ, Bilkent, Koç, Sabancı, Yeditepe, Kocaeli, Uludağ, Erciyes, Dokuz Eylül, Ankara University ◄
► **Visiting scientist** at Intersil & UC Santa Cruz in Summer 2006. Invited for a lecturer position to UC San Diego CS Department in Summer 2007
Helped Bahçeşehir seniors become **TA/RAs** at CWRU (1), Northeastern (3), Oakland (5), Ohio St. (1), UMass Lowell (2), UIC (1), Univ. of Arizona (1) ◄
► Placed top Bahçeşehir **alumni** in **jobs** at ST-Ericsson (4), Vestel Vestek (4), Vistek ISRA (1) all in İTÜ Teknokent, Eti Makina (1), Votel (1)

EMPLOYMENT HISTORY

Assistant Professor at **Özyeğin** University, İstanbul, Sep **2010** – Present
Assistant Professor at **Bahçeşehir** University, İstanbul, Dec **2004** – Sep **2010**
Staff Hardware Design Engineer at **Nvidia**, Santa Clara, CA, USA, Apr **2004** – Oct 2004
Senior Systems Architect at **ARC** International, San Jose, CA, USA, Mar **2003** – Mar 2004
Staff Design Engineer at **failed start-ups**, SF Bay Area, CA, USA, Feb **2002** – Jan 2003
Staff Design Engineer at **Juniper Networks**, Sunnyvale, CA, USA, Jan **2001** – Feb 2002
Distinguished MTS at **Lucent** Microelectronics, Santa Clara, CA, USA, Sep **1997** – Jan 2001
Engineer/Specialist at **General Motors** R&D Center, Warren, MI, USA, Mar **1993** – Aug 1997
Machine Vision Engineer at **General Electric**, Cleveland, OH, USA, Jun **1989** – Oct 1992

EDUCATION

PhD in EE, Jan **1995, Case Western Reserve University,** Cleveland, OH, USA (GPA: 4.00/4.00)
Dissertation on VLSI CAD, Retiming, Parallel Microarchitectures. Led by Prof. Christos A. **Papachristou**. Supported by NASA as an **RA**.

MS in EE, May **1989, Case Western Reserve University,** Cleveland, OH, USA (GPA: 4.00/4.00)
Thesis on Machine Vision for Robotics. Led by Prof. Francis L. **Merat**. Supported by CWRU as a **TA**.

BS in EEE & Physics (double major), Jul **1986, Boğaziçi University**, İstanbul (GPA: 3.76/4.00) ***Top Graduate***
Senior Project on Adaptive Baseband Equalization for Digital Communications. Led by Prof. Ömer **Cerid**.

HONORS & AWARDS

Innovation Award, Intersil Corporation, Milpitas, CA, USA, Nov 2006 (with Dr. Iskender Agi)
Distinguished Member of Technical Staff, Lucent Microelectronics, Santa Clara, CA, USA, Apr 1999
McCuen Award, General Motors R&D Center, Warren, MI, USA, Jun 1996 (with Tom E. Fuhrman)
Acknowledged by Professor Donald Thomas of Carnegie-Mellon University in his popular **Verilog** book starting in the 1996 edition
Panelist in panel: *Is High-Level Synthesis Marketable?*, 7th International Symp. on High-Level Synthesis, Ontario, Canada, May 1994
Was offered a faculty position in the CMPE Department at **Boğaziçi** starting in Sep 1993
The **only** student to pass the PhD Comprehensive exam in the EE Department at Case Western Reserve in Fall 1988
Ranked **1st** in all of the graduating class at **Boğaziçi** University (including all faculties) in 1986
Ranked **3rd** nationwide in the second leg of **ÖSS** in 1982 among 408,000 examinees
Top **2nd** place in both Physics and Math competitions of TÜBİTAK in Central Anatolia at high school level in 1982

ACADEMIC EXPERIENCE

Assistant Professor, Electrical and Electronics Engineering (EEE), **Özyeğin** University, İstanbul, Sep 2010 – Present
Adjunct Faculty Member, Computer Engineering (CMPE), **Özyeğin** University, İstanbul, Sep 2010 – Present
Assistant Professor, CMPE, **Bahçeşehir** University, İstanbul, Aug 2008 – Sep 2010
Adjunct Faculty Member, EEE, **Bahçeşehir** University, İstanbul, Aug 2008 – Sep 2010
Grad. Program Coordinator, Embedded Video Systems (under MS-EEE & CMPE), **Bahçeşehir** University, İstanbul, Jun 2008 – Present
Associate Chairman, Computer Engineering, **Bahçeşehir** University, İstanbul, Sep 2008 – Aug 2009
Adjunct Faculty Member, Physics, **Boğaziçi** University, İstanbul, Feb 2004 – Jan 2009
Assistant Professor, Electrical and Electronics Engineering, **Bahçeşehir** University, İstanbul, Dec 2004 – Jul 2008
Visiting Faculty, Computer Engineering, **University of California**, Santa Cruz, CA, USA, Jun 2006 – Sep 2006
Adjunct Faculty Member, Mechatronics Engineering (MCH), **Bahçeşehir** University, İstanbul, Sep 2005 – Aug 2006
Research Assistant, Computer Engineering, **Case Western Reserve** University, Cleveland, OH, USA, Sep 1990 – Feb 1993
Research Assistant, Economics, **Case Western Reserve** University, Cleveland, OH, USA, Nov 1990 – May 1991
Teaching Assistant, Electrical Engineering, **Case Western Reserve** University, Cleveland, OH, USA, Aug 1986 – May 1989

ACADEMIC SERVICE

Teaching

Always used a web page (on ugurdag.com) and a YahooGroup (with email archiving, polls, and more) for my courses
Authored original test questions for all my courses reaching hundreds for courses I frequently teach
Created software tools that can automatically create web pages from a list of questions
Introduced real engineering projects into Digital Design course with PIC based design tasks in addition to FPGAs
Frequently included software projects (esp. in data compression) with web-based automation in upload and correlation
Always received high evaluation scores and comments from students at the end of semesters (between 75% and 100%)

Taught the following courses:

sophomore/junior-level **Digital Design** (with an FPGA/Verilog based lab) 10 times since Fall '05 (to EEE & MCH)
junior-level **Data Communication Standards** 6 times, every Spring since '05 (to CMPE, in 2 sections)
sophomore-level **Circuit Theory** in Fall '05 and Spring '11 (to EEE)
senior-level **Digital IC Design** in Spring and Fall '05 (to CMPE, EEE)
sophomore-level **Digital System Design Lab** (based on FPGAs and Verilog) in Spring '06 and '07 (to CMPE)
junior-level **Operating Systems** in Fall '06 and '07 (to CMPE & Math/CS, in 3 sections)
grad-level **Machine Vision** course in Fall '06
grad-level **Industrial Automation** course in Spring '07
senior-level **Pillars of Computing** course in Spring '04, in Fall '07, in Fall '08
grad-level **HDL-based Design Project** course (i.e., Advanced IC Design) 4 times since Fall '05
grad-level **Digital Design Automation and Compilers** course in Spring '06
grad-level **Computer Arithmetic** course in Fall '08
grad-level **ASIC/SOC Design** course in Fall '09
grad-level **Embedded Systems Design** course in Fall '10
grad-level **Computer Architecture & Performance** course in Spring '11
grad-level **Hardware Design Patterns** course in Summer '11

New Programs & Partnerships

Established a graduate program module called **MSEVS** (Embedded Video Systems) in EEE & CMPE at Bahçeşehir in collaboration with Vestel Vestek
As the program coordinator, admitted 28 students to MSEVS in 2 yrs. Most were **top** students in their class (see ugurdag.com)
Univ. rep. are **İTÜ**, Bilkent, Koç, Sabancı, Yeditepe, Kocaeli, Uludağ, Erciyes, Dokuz Eylül, Ankara U., Gaziantep U., Kadir Has, Marmara, Bahç.
Some of the above students worked at **companies** such as Vestel Vestek, ST Microelectronics, Vistek ISRA, Ulaşım AŞ, Votel, Airties
Helped establish an undergraduate program/dept. in **Mechatronics** Engineering at Bahçeşehir Univ.
Was instrumental in forming a collaboration between TelkoDer & Bahç. to establish an eng. management. MS program called **TelekomLiderleri**
Signed up ST Microelectronics (now called ST-Ericsson), YemekSepeti, and Votel in Bahçeşehir **Coop** Program
Liaison for Bahçeşehir's joint 3+2 BS/MS programs with **Cleveland State University** in CMPE, EEE, and Biomed (with Cleveland Clinic)
Organized a round-table in May '06 at Bahçeşehir, called **Istanbul Chip Summit,** moderated by Professor Duran Leblebici
The round-table had **representation** from ST, Maxim, CMOSvision, Airties, TÜBİTAK-UEKAE, Koç, Sabancı, Yeditepe, Yıldız

Labs Established

In the process of establishing an **Embedded Systems Lab** at Özyeğin with donations from TI
Established a **VLSI/FPGA Design Lab** at Bahçeşehir with 50+ boards, several SW tools, 25 seats, and 15 PCs, which served ~800 students in 5 yrs
Helped establish an **Embedded Systems Lab** with ~30 boards (Gumstix, FriendlyArm, Ebox), serving ~100 students per semester since 2009
Helped establish a **Robotics/Vision Lab** (a project only lab), bought Lego Mindstorms kits, DVT/Cognex and Matrox vision systems

Helped establish an **Automation Lab**, had a big and a small conveyor belt system, 2-axis gantry robot, and a bottle-filling machine built

Competitions, Team/Club Building & Mentoring

Organized a training camp for high school students called **Robokamp** at Özyeğin, with contributions from FordOtosan, ABB, Altınay Robotics
Started Bahçeşehir Robotics Team with **RoboCamp** in Summer 2005 and acted as their advisor since then
They won many **awards** including ones at İTÜro, ODTÜ, Boğaziçi, Bilkent, MEB, Doğuş, Uludağ, Sakarya
The team (which later transformed into Mechatronics Club) used the previously mentioned **Robotics/Vision Lab** as a playground
Closely guided students on **TeamSumo** and **Virtual SmartBoard** (resulted in a patent filing) projects and won awards at İTÜro and Doğuş
Was an advisor to the **Solar Car Team**. They participated in TÜBİTAK's Solar Car Race twice and placed in the top ten
Advisor to **IEEE Engineering & Technology Club**. Helped them get established and organized many activities/seminars with them
Mentored a team of 4 CMPE seniors in Spring 2008 that qualified for **Microsoft Imagine Cup** with their project on a novel navigation sys.

Miscellaneous Service

Formed the **CMPE Industry Advisory Board** with rep. from Alcatel/Lucent, TT/Argela, Grid, IBM, Intel, Logo, Microsoft, ST, Vestel, YemekSepeti
Worked on revision of the **curricula** of CMPE & EEE departments
Led the **web page development** efforts at the School of Engineering on an on-and-off basis
Played an important role in **TA hiring** in CMPE, EEE, and MCH departments between 2005-09
Traveled to Mersin, Adana, Gaziantep, Keşan, and locally within İstanbul to **promote** Bahçeşehir engineering programs
Gave **presentations** introducing Bahçeşehir School of Eng. and the university as a whole to a delegation from Intel EMEA and a US Think-Tank
Organized **countless talks** (some with the IEEE Student Chapter) with audiences of anywhere from 10 to 300+
Some **talks** were research talks, some on technology at a layman level, some on job hunting, and some on finding scholarships abroad
Organized student and faculty member **field trips** to companies and factories

Conference Organization & Program Committee Work

General co-Chair (planned), 21st IFIP/IEEE/ACM Intl. Conf. on VLSI and System-on-Chip (**VLSI-SoC**), **İstanbul**, Oct **2013**
Publicity Chair, 9th IEEE/ACM/IFIP Intl. Conf. on High Performance Computing & Simulation (**HPCS**), İstanbul, **Turkey**, Jul **2011**
Program Comm. Member, 23rd IFIP/EEE/ACM Symp. on Integrated Circuits and Systems Design (**SBCCI**), São Paulo, **Brazil**, Sep **2010-11**
Intl. Liaison, 8th IEEE/ACM/IFIP Intl. Conf. on High Performance Computing & Simulation (**HPCS**), Caen, **France**, Jun **2010**
Program Comm. Member, 10th–14th Conf. on Trends in the Dev. of Machinery and Assoc. Tech. (**TMT**), **Turkey/Tunisia/Bosnia/Spain**, Sep **2006-10**
Program Comm. Member, 2nd–5th IEEE/ACM NASA/ESA Conf. on Adaptive Hardware and Systems (**AHS**), **Holland/UK/USA**, Jun **2007-10**
Program Comm. Member, 3. Ağ ve Bilgi Güvenliği Ulusal Sempozyumu (**ABGS**), Ankara, Feb **2010**
Local Organizing Comm. Member, 1st IEEE/ACM NASA/ESA Conf. on Adaptive Hardware and Systems (**AHS)**, **İstanbul**, Jun **2006**
Local Organizing Comm. Member, 9th Conf. on Trends in the Development of Machinery and Associated Technology (**TMT**), **Kemer**, Sep **2005**

Project & Paper Refereeing

Qualification stage referee of KOSGEB projects (at IMES), reviewed close 30 projects in 4 panels so far
Qualification stage referee for 11 **TÜBİTAK-TEYDEB** projects with budgets of $120k-$600k in the areas of IC, HW, SW, and system design since 2007
Monitoring stage referee of 3 TÜBİTAK-TEYDEB projects on IP-TV, IC Design, and ERP SW
Qualification and monitoring stage referee for a **TÜBİTAK-1007** project with a $2M budget in the area of Public Resource Planning SWs since 2008
Qualification stage referee for a **TTGV** project with a $2M budget in the area of FPGA-based HW accelerators in 2007
Reviewer for TÜBİTAK's **Turkish Journal of Electrical Engineering and Computer Sciences** since 2010
Reviewer for **Elsevier Computers & Operations Research Journal** since 2008
Reviewer for **IEEE Transactions on VLSI CAD** in 1991–92
Reviewer for IEEE Intl. Conference on Field-Programmable Technology (**FPT**) in 2011
Reviewer for IEEE Intl. Conference on Electronics, Circuits, and Systems (**ICECS**) in 2008 and 2011
Reviewer for IEEE Intl. Symposium on Mechatronics and its Applications (**ISMA**) in 2008 and 2010
Reviewer for IEEE Intl. Symposium on Circuits and Systems (**ISCAS**) in 2006
Reviewer for IEEE/ACM Design Automation Conference (**DAC**) between 1994–96

Student Advising

Acted as the official academic advisor of **100+** CMPE, EEE, and MCH students so far (mostly undergrad)
Helped most **throughout** their enrollments at Bahçeşehir
Overtook **problem students** nobody else would and saw a good number of them graduate
Mentored and officially or **unofficially** advised many bright students
Helped Bahçeşehir seniors become **TA/RAs** at Case Western (1), Northeastern (3), Oakland (5), Ohio State (1), UMass Lowell (2), UIC (1)
Only half the students above are in my fields of research. I guide students in the right direction in fields as far as communications and data mining
3 of them went to study VLSI, 3 Embedded Systems, 1 Power Systems, 4 Data Mining, 2 Industrial Engineering
Helped one top Bahçeşehir senior get a Board of Trustees scholarship and do an MS at **Stanford** (he is now working at Cisco in Silicon Valley)
Provided guidance to a Bahçeşehir senior while she got a **Fulbright** scholarship and went to **USC** for an MS in CS to study Computer Graphics

Sent 2 top students to **Boğaziçi** for **PhD**, 1 to CMPE to study digital systems and IC design, 1 to EEE to study Robotics/Vision
Sent 4 top students to **Boğaziçi** for **MS**, 2 to CMPE to study Computer Vision and Networking, 2 to EEE to study Robotics/Vision and Telecom
Sent 1 top student to **İTÜ** for MS in CMPE to study cryptography
All 7 students above are supported by **TÜBİTAK-BİDEB** scholarships or **TÜBİTAK-1001** funding
Helped top Bahçeşehir students land **jobs** at ST-Ericsson (4), Vestel Vestek (4), ISRA Vistek (1), TÜBİTAK (2), Grid (1), Huawei (3), Mobinex (2)
Helped many students find internships, paid part-time jobs, and free-lance work
Always kept an open-door policy for students from **all over Turkey** that aspire to become chip & embedded systems designers
In the course of doing that, had the chance to advise students from Boğaziçi, İTÜ, ODTÜ, Bilkent, Sabancı, Yeditepe, TOBB, Erciyes
Was instrumental during the process in which a Boğaziçi EEE senior got an RAship from **MIT** in the field of Robot Vision in 2008
Was instrumental during the process in which an Erciyes EEE PhD student got a research eng. position at **MIT** in 2007, a postdoc at **Bilkent** in 2011
Was instrumental during the process in which a Boğaziçi MS graduate and a Boğaziçi MS student got TAship from **UC San Diego** in 1996

Completed MS Theses

Hatice Şahin, in Sep 2011, Bahçeşehir EEE, on **HW Design for Numerical Processing**
Okan Keskin, in Sep 2010, Bahçeşehir EEE, on **Carry Save Tree** Generation
V. Uğur Güney, Jun 2010, Boğaziçi Physics, "Triggerless Particle Identification Systems using **FPGA**" (co-advised)
Onur G. Öcal, Apr 2010, Bahçeşehir EEE, "**2.5-Axis** Semi-Virtual Plotter"
Coşkun Kazma, Aug 2009, Bahçeşehir CMPE, "MC2MV: MicroController driven **Motion Control** & Machine Vision assisted sorting system"
Ferhat Canbay, Jul 2009, Bahçeşehir CMPE, "Point based Correspondenceless **Pose Estimation**" (co-advised)
Erinç Topdemir, Sep 2008, Bahçeşehir EEE, "Team Sumo [**Robots**]"
Onur Başkirt, Jun 2008, Bahçeşehir EEE, "New Logic Architectures for **Round Robin Arbitration** and their Automatic RTL Generation"
Soner Dedeoğlu, Jan 2008, Bahçeşehir CMPE, "HW Implementation of True-**Motion Estimation** with 3D Recursive Search Block Matching Algorithm"

Ongoing MS/PhD Theses

Ayhan Yanarsoy, PhD expected in Jun 2015, Özyeğin EEE, on VLSI CAD **Automation**
Ali Başaran, MS expected in Jan 2012, Bahçeşehir EEE, on **FPGA** based DAQ System Design
Özgür Özkurt (co-advised), MS expected in Jan 2012, Bahçeşehir EEE, on **Secure HW** Design with FPGAs
Abdullah Yıldız (co-advised), MS expected in Jan 2012, Özyeğin EEE, on **Secure HW** Design with FPGAs
Anıl Bayram, MS expected in Jan 2012, Bahçeşehir EEE, on **Computer Arithmetic**
Fatih Temizkan, MS expected in Jun 2012, Özyeğin EEE, on **Computer Arithmetic**
Gökhan Güner, MS expected in Jun 2013, Özyeğin EEE, on **4G** HW Design using FPGAs
Bilgiday Yüce (co-advised), MS expected in Jun 2013, Boğaziçi EEE, on **Digital System Design**
Okan Palaz, MS expected in Jun 2013, Özyeğin EEE, on **Video Compression HW Design**

Completed Senior Projects

8 Senior projects on **FPGA/VLSI design** and **Computer arithmetic**
17 Senior projects on **Industrial automation** and **Embedded systems**
12 Senior projects on **Computer vision** and **Robotics**
27 Senior projects on **Software automation** of a variety of tasks including attendance entering to automated grading of software tests

Invited Talks

"Opportunities in doing PhD on VLSI in the USA", School of Engineering at Erciyes University, Kayseri, May 2011
"FPGA Design", Computer Engineering Department at Marmara University, İstanbul, May 2010
"A VLIW Architecture Based on Shifting Register Files", Computer Engineering Department at Boğaziçi University, İstanbul, Nov 1992
"A VLIW Architecture Based on Shifting Register Files", Computer Engineering Department at ODTÜ, Ankara, Nov 1992
"A VLIW Architecture Based on Shifting Register Files", Computer Engineering Department at Bilkent University, Ankara, Nov 1992

ONGOING AND FUTURE RESEARCH

(See end of the CV for a Publication List)

Embedded Systems

Intrusion Detection on High-Speed Train Tracks: With Bahçeşehir **UYGAR** (Prof. Mustafa Ilıcalı) & **TCDD**.
Congestion driven Navigation: Navigation device sends back data to allow discovery of congestion. (Microsoft Imagine Cup Semi-Finalist in 2008)
Student Attendance Taking with a Handheld Device: Cost optimized embedded and portable device takes attendance using RFid & fingerprints.
MQT: stands for Merchandise Query Terminal. Will find use in supermarket aisles and offer query, navigation, digital signage, and coupons.
Team-Sumo: Robot teams compete with each other using artificial intelligence, wireless, and computer vision technologies.
3D Scanner: Based on a camera plus a line-laser. Uses our pose estimation algorithms for calibration.

Software Automation

Bus Arrivals: SW-prototype running on iPhone. It uses Google Maps API and lets the user pick a bus-stop and see a list of buses and arrival times.
Cab Call Center: All cab stations are centralized into a single virtual cab station. SW-prototype uses GPS data with Google Maps API.
ASCPE: stands for Automated Software Coding Proficiency Exam. Administers coding tests and their grading – all automated. Like codechef.com.
Digital Signage: In conjunction with my consulting work at Vizyonik. Our patent-filed advertising media needs special digital signage SW.
Facebook Application for Alumni Org.s: Keeping alumni DBs up-to-date is a problem. Linking it to Facebook is key. Early adopters: Bahç. & Boğ.
sQ: means Smart Question. The concept is to store ÖSS questions & alike as dynamic questions that expand into 100s of questions. 1 conf. paper.
Student Tickers: is a (web-based) system/methodology. Speeds up attendance/score entering. Students are rep. by ticker symbols

Computer Arithmetic

Round Robin Arbiters: Planning to submit a journal paper on it in October 2011.
Carry Save Trees: Had an MS thesis completed on it with applications in Saturated Unsigned Adders. 1 conf. paper so far.
Exponentiation: Had an MS thesis completed on it. The deliverable will be a software that generates fast and small circuits.
Other problems in the pipeline are **Divide by constant** and **Series of multiplications**.

VLSI CAD

ACTreS: Spent time on an Analog Clock Tree Synthesis tool while at Intersil (in Silicon Valley) in Summer 2006. Doing a TÜBİTAK-1001 project on it.
Mapping Tools for Nanocrossbars: Led by Dr. Sezer Gören Uğurdağ. So far produced 2 conf. papers, 1 submitted journal paper.
HDLtk: Spent time on dev. of an HDL toolkit with Dr. Sezer Gören Uğurdağ while at UC Santa Cruz in Summer 2006. Will resume efforts in a year.
AutoCircuit: is a High-Level Syn. tool I developed at GM R&D. A company licensed our SW and I was allowed to publish 1 conf. paper.
Scheduling in Pipelined Systems: Was part of my PhD dissertation. Produced 5 conf. papers, and 1 journal in EJOR (a class). May go back to it.

FPGA/ASIC Design and HW Friendly Algorithm Development

PUF: Investigating using Physically Unclonable Functions for FPGA design security. Led by Dr. Sezer Gören Uğurdağ. 3 conf. papers so far.
GPF: Working on a novel FPGA architecture, called Gigahertz Pulse Fitter, for a DAQ problem jointly with Boğaziçi within a TÜBİTAK-1001 project.
Communications: Collaborative work on HW friendly coding algorithms (1 journal paper). A new collab. will be on HW impl. of MIMO power alloc.
Video Compression: Working with Vestel Vestek on new embedded video compression algorithms (and their impl.) for DRAM bandwidth reduction.

Computer Vision

Pose Estimation: was my MS research area. Recently produced a journal paper on it with Dr. Sezer Gören Uğurdağ.

CONSULTANCY

Vestel Vestek, Turkey, May 2007 – Present: Serving Pixellence Grp. in design of video enhancement FPGA/ASIC proj.s, esp., FRC and effects engine.
Vizyonik, Turkey, Jan 2007 – Present: Worked on a mach. vision proj. at Borusan. Now working on design of novel advertising media. Patents filed.
TCDD, Turkey, Nov 2009 – Feb 2010: With my team of 3 engineers compiled a spec doc. for ntwk & computer vision part 200km security system bid.
Iontek, Turkey, Jan – Mar 2009: Helped them with an Nvidia CUDA version of their bioinformatics SW within a TÜBİTAK-TEYDEB project.
Synplicity, Turkey, Nov 2006 – Feb 2007: Helped them with their DSP synthesis tool. (Synplicity, a US firm, is now part of Synopsys.)
FordOtosan, Turkey, Jun – Dec 2006: Was part of a team from İTÜ-OTAM that designed a test system for FordOtosan for their truck engine project.
Intersil Corporation, USA, Jun – Sep 2006: Did the ground work for ACTreS (see Research section above), which we later proposed as a 1001 proj.
Aspendos Communications, USA, Jan – Jun 2002: Acted as a liaison for the new start-up. My efforts resulted in an extra $1M funding from USVP.
Visionex, USA, Nov 1996 – Apr 1997: Sold the idea of a machine vision system to Lüleburgaz plant of ŞişeCam. Also helped with engineering.

INDUSTRY EXPERIENCE

***Staff Hardware Design Engineer at Nvidia*, Santa Clara, CA, USA, Apr 2004 – Oct 2004**
Worked on methodology and delivery issues of 3D graphics and video codec cores to major US and European semiconductor and wireless companies. Interfaced with the RTL design group. Turned the design from an internally used block to a portable IP. Interacted with an overseas customer over teleconferencing and site visits. Participated in pre-sales meetings with potential customers and Nvidia higher management.

***Senior Systems Architect at ARC International*, San Jose, CA, USA, Mar 2003 – Mar 2004**
Was responsible for project management and design of test chips. Implemented a 0.18 micron and 750K gate SOC. The chip had 2 ARC processors, Ethernet, USB, UART, GPIO, off-chip memory, and bus interfaces. Interacted with Chip Express for the chip's implementation as a structural ASIC. Did chip-level synthesis and spent time on precise timing of certain pins that interface to asynchronous off-chip components. ARC (now part of Virage Logic) makes chip building blocks for embedded systems in various market segments such as consumer electronics, wireless devices, networking, and media gateways.

***Staff Design Engineer at failed start-ups*, SF Bay Area, CA, USA, Feb 2002 – Jan 2003**
Worked with multiple start-up companies on 20M+ gate chips. At Teradiant Networks, worked on a packet processor and did verification and synthesis. At Pulsent, worked on a proprietary model based video compression chip and did RTL design as well as architectural work for a processor (and its

interface) that does non-timing critical work outside the regular video pipeline. At Chameleon Systems, worked on next-generation reconfigurable chips (based on DSP slices) for wireless base stations and video encoders.

***Staff Design Engineer at Juniper Networks*, Sunnyvale, CA, USA, Jan 2001 – Feb 2002**

First worked on a "packet spray" chip. Later worked on a packet processor with multiple 10G interfaces. Personally worked on the results processor block. Block had a size of 650K gates and was part of a 20M gate 0.13 micron chip. Used HDL generation methodology with Perl for quick RTL development. The block put packets back in order -- Cisco was making bad publicity due to this problem. Fixed the problem with a novel systolic array architecture. Worked with higher management and software guys for feature definition. Also worked with the designers of neighboring blocks for protocol definition of internal interfaces. Worked with a dedicated module verification engineer as well as system verification people.

***Distinguished MTS at Lucent Microelectronics*, Santa Clara, CA, USA, Sep 1997 – Jan 2001**

Initially was an MTS in an ASIC services group. In that position, was stationed at Apple Computer doing synthesis for 3-4 months. Was involved in 3 chips with Apple. Was the owner of USB IP that went from Lucent to Apple in the 2nd chip. In all 3 chips Lucent was the ASIC vendor. While owning the USB IP, got involved in RTL changes. In this ASIC position, also did verification, DFT, functional test vector development & verification, ground bounce analysis, timing, floorplanning, and more. In May 1999, transferred to a standard products group doing an HPNA 2.0 (Ethernet over phone-line) chip. Designed half the chip (150K gates & 9K lines of RTL) single handedly and helped with rest of the chip including verification and algorithm development. Used Verilog code generation methodology from Perl. Created the Perl infrastructure for that from scratch. This methodology kept the source code of the design in Perl. 1,500 lines of Perl generated 9,000 lines of RTL within a few minutes. With this methodology, one could respond to algorithmic changes made by the fixed-point guys in a day, including design changes as well as full verification. Interacted closely with the fixed point engineers. Designed an optimized sine LUT using some math and Perl. In April 2000, got promoted to Distinguished MTS and started directly reporting to the director. In this position, hired one engineer and developed a floating/fixed point methodology (a C++ library with operation overloading) as well as a simulation infrastructure involving Verilog API for co-verification of C++ fixed point algorithms and RTL.

***Engineer/Specialist at General Motors R&D Center*, Warren, MI, USA, Mar 1993 – Aug 1997**

Worked on AutoCircuit (AC) – one of the first behavioral synthesis tools with silicon success. I did both algorithm development and software implementation. Delphi (then GM Delco) used AC for several ASICs including XM satellite radio. AC allowed the designer to code in a higher level Verilog than regular RTL with multiple clock cycles in an always block and place clock edges almost anywhere. This let the designer to code directly in an algorithmic style. AC had superior resource sharing algorithms. It had novel and powerful mux sharing/optimization techniques as well as novel memory inference capabilities. AC could dump RTL or structural Verilog with high-level datapath components, which could be fed to Cascade Design Automation's Epoch physical design tool. DAsys (a start-up from Carnegie-Mellon) later licensed AC and its source code and commercialized it with successful customer interactions at ATI and elsewhere. DAsys got bought by Cynapps, which later got snapped by Forte Design Automation. AC may still have its remnants in Forte's Cynthesizer tool. AC also influenced the formation of Chameleon Systems (which I later joined).

***Machine Vision Engineer at North Coast Automation*, Cleveland, OH, USA, Jun 1989 – Oct 1992**

Designed machine vision systems for industrial inspection and quality control applications at General Electric plants. Worked on feasibility studies, optical set-up design, formalizing measurement methods, algorithm design, software development, installation, test, and troubleshooting. Algorithms had to be real-time with usually less than 200ms run-time on super-slow processors in today's standards (at max 33MHz). Worked full-time until Sep 1990 and part-time afterwards. Worked on about 10 projects and wrote nearly 50 thousand lines of code in C.

PATENT APPLICATIONS

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